

CMOS 16-BIT HIGH-SPEED MICROPROCESSOR SLICE

KEY FEATURES

- **Four CMOS 2901 Type Devices in a Single Package**
- **On Board Look-Ahead Carry Generator**
- **Low CMOS Power**
— 225 mW
- **High Speed Operation**
— 50 ns Read-Modify-Write
- **Fully Firmware Compatible with the Bipolar Device Configuration of Four 2901s and One 2902A**

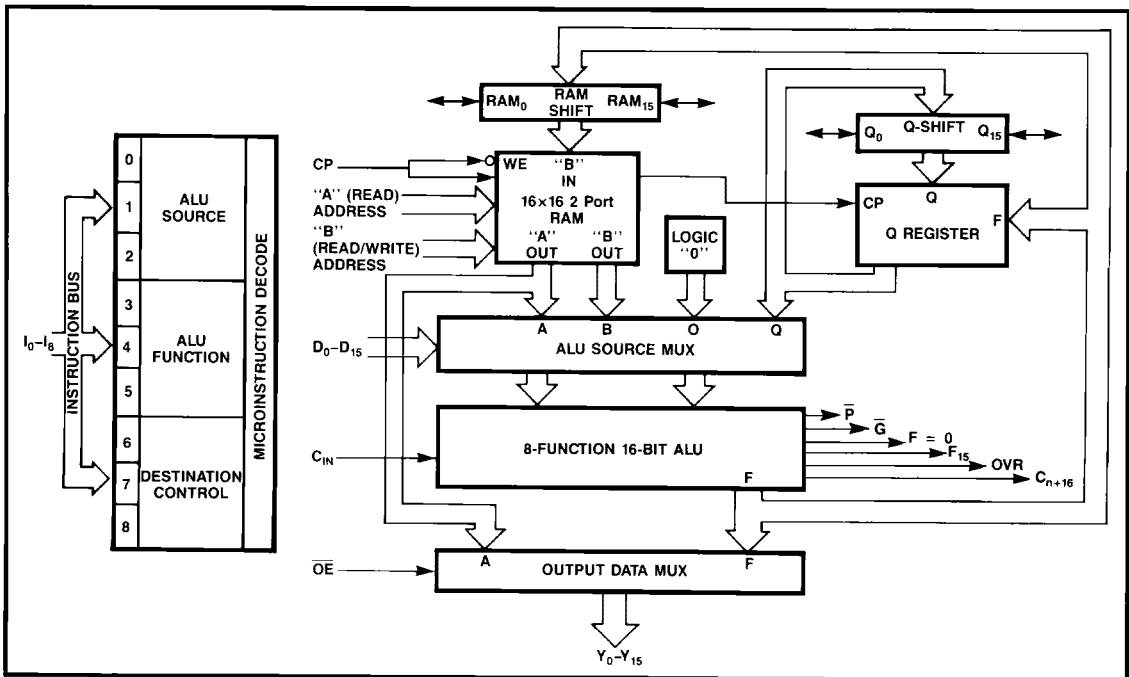
GENERAL DESCRIPTION

The WS59016 is a 16-bit high-speed microprocessor which combines the functions of four 2901 4-bit slice processors and distributed look-ahead carry generation on a single High Performance CMOS device.

This microprogrammable circuit has the flexibility to efficiently emulate almost any digital computing machine. It is an ideal candidate for such applications as peripheral controllers, CPUs, programmable microprocessors, and Digital Signal Processors.

The advanced CMOS process, with which the WS59016 is manufactured, provides significant performance improvements over an equivalent Bipolar device configuration. While operating faster than a 2901C based system, the WS59016 requires less than 3% of the power consumed by an equivalent Bipolar system.

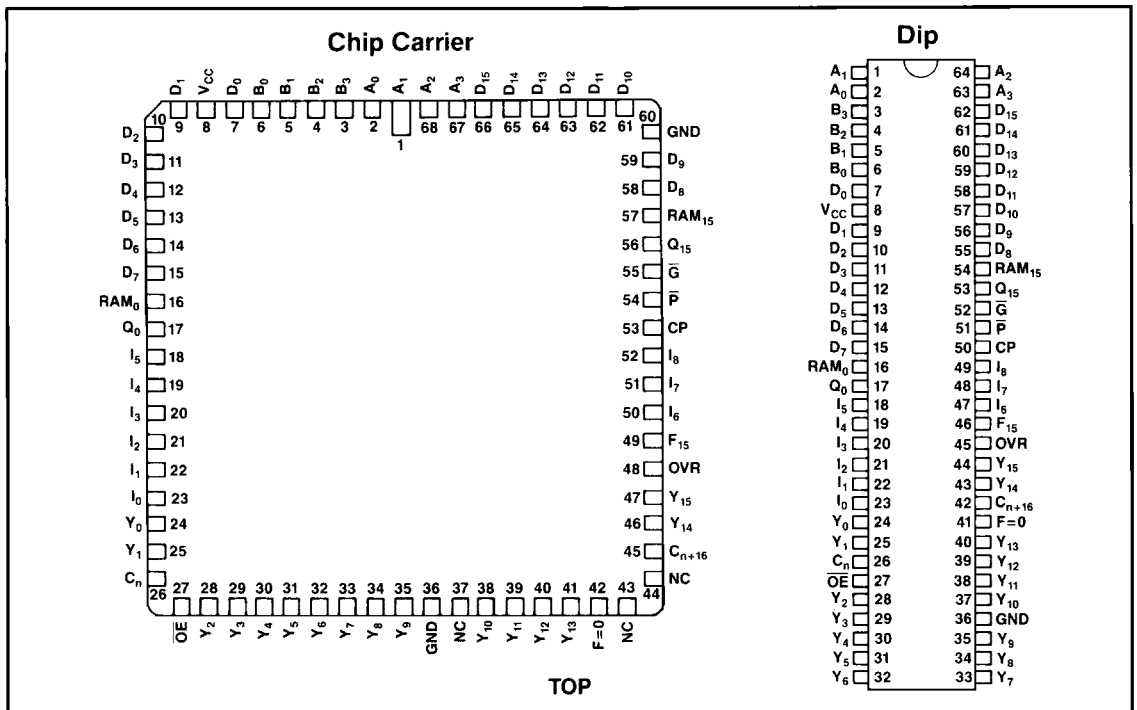
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

| Signal Name | I/O | Description |
|---------------------------------|-----|--|
| A0-3 | I | Addresses which select the word of on board RAM which is to be displayed through the A port. |
| B0-3 | I | Addresses which select the word of on board RAM which is to be displayed through the B port and into which data is written when the clock is low. |
| I0-8 | I | Block of three instruction groups which are to select 1) which data sources will be applied to the ALU (I012), 2) what function the ALU will perform (I345), and 3) what data is to be written into the Q register or on board RAM(I678). |
| Q15, RAM15 | I/O | Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I678 indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the ALU output is available on the RAM 15 pin and the MSB of the Q-register is available on the Q15 pin. Otherwise, the pins appear as inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of RAM (octal 4 and 5) and the Q register (octal 4). |
| Q0, RAM0 | I/O | Shift lines similar to Q15 and RAM15, however the description is applied to the LSB of RAM and the Q-register. |
| D0-D15 | I | These sixteen direct data inputs can be selected as a data source for the ALU. D0 is the LSB. |
| Y0-Y15 | O | These sixteen three state outputs, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I678. |
| \overline{OE} | I | When high, the Y outputs are in the high impedance state. When low, either the contents of the A-register or the outputs of the ALU are displayed on Y0-Y15, as determined by I678. |
| \overline{G} , \overline{P} | O | The carry generate and propagate outputs of the ALU. |
| OVR | O | This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation. |
| F = 0 | O | This output, when high, indicates the result of an ALU operation is zero. |
| F15 | O | The most significant ALU output bit. |
| Cn | I | The carry-in to the ALU. |
| Cn + 16 | O | The carry-out of the ALU. |
| CP | I | This clock signal is applied to the A and B-port latches, RAM, and Q-register. The clock low time is the write enable to the on-board dual port RAM, including set-up time for the A and B-port registers. The A and B-port outputs change while the clock is high. The Q-register is latched on the clock low-to-high transition. |

PIN ORIENTATION



ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) 0°C to +70°C
 (Mil) -55°C to +125°C
 Storage Temp. (No Bias) -65°C to +150°C
 Voltage on Any Pin with
 Respect to GND -0.6V to +7V
 Latch-Up Protection >200 mA
 ESD Protection > ±2000V

*Notice: Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC READ CHARACTERISTICS Over Operating Temperature Range (Note 1)

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN | MAX | UNITS |
|-----------------|-------------------------------|---|-----------------------|--------------------------------|-----|-------|
| V _{OH} | Output High Voltage | V _{CC} = Min V _{IN} = V _{IH} or V _{IL} | All Outputs | I _{OH} = -3.4 mA | 2.4 | V |
| V _{OL} | Output Low Voltage | V _{CC} = Min V _{IN} = V _{IH} or V _{IL} | All Outputs | I _{OL} = 12 mA Comm'l | 0.5 | |
| | | | | I _{OL} = 8 mA Mil | | |
| V _{IH} | Input High Voltage | Guaranteed Input High Voltage | | 2.0 | | |
| V _{IL} | Input Low Voltage | Guaranteed Input Low Voltage | | 0.8 | | |
| I _{IX} | Input Load Current | V _{CC} = Max, V _{IN} = Gnd or V _{CC} | | -10 | 10 | μA |
| I _{OZ} | High Impedance Output Current | V _{CC} = Max, V _O = Gnd or V _{CC} | | -50 | 50 | |
| I _{CC} | Power Supply Current | V _{CC} = Max | Comm'l (0°C to +70°C) | | 45 | mA |
| | | | Mil (-55°C to +125°C) | | 60 | |

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C. 2) Military: V_{CC} = +5V ± 10%, T_A = -55°C to +125°C.

LOGIC FUNCTIONS FOR \bar{G} , \bar{P} , C_{n+16}, and OVR

The four signals \bar{G} , \bar{P} , C_{n+16}, and OVR are designed to indicate carry and overflow conditions when the WS59016 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

Definitions

$P_i = R_i + S_i$
 $G_i = R_i \cdot S_i$
 $P_{0-3} = P_0 \cdot P_1 \cdot P_2 \cdot P_3$ $G_{0-3} = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0$
 $P_{4-7} = P_4 \cdot P_5 \cdot P_6 \cdot P_7$ $G_{4-7} = G_7 + P_7 \cdot G_6 + P_7 \cdot P_6 \cdot G_5 + P_7 \cdot P_6 \cdot P_5 \cdot G_4$
 $P_{8-11} = P_8 \cdot P_9 \cdot P_{10} \cdot P_{11}$ $G_{8-11} = G_{11} + P_{11} \cdot G_{10} + P_{11} \cdot P_{10} \cdot G_9 + P_{11} \cdot P_{10} \cdot P_9 \cdot G_8$
 $P_{12-15} = P_{12} \cdot P_{13} \cdot P_{14} \cdot P_{15}$ $G_{12-15} = G_{15} + P_{15} \cdot G_{14} + P_{15} \cdot P_{14} \cdot G_{13} + P_{15} \cdot P_{14} \cdot P_{13} \cdot G_{12}$
 $C_{n+15} = G_{12-14} + P_{12-14} \cdot G_{8-11} + P_{12-14} \cdot P_{8-11} \cdot G_{4-7} + P_{12-14} \cdot P_{8-11} \cdot P_{4-7} \cdot G_{0-3}$
 $P_{12-14} = P_{12} \cdot P_{13} \cdot P_{14}$ $G_{12-14} = G_{14} + P_{14} \cdot G_{13} + P_{14} \cdot P_{13} \cdot G_{12}$

| I ₅₄₃ | Function | \bar{P} | \bar{G} | C _{n+16} | OVR |
|------------------|-------------------------|---|---|------------------------|---------------------------------------|
| 0 | R + S | $\overline{P_{0-3} \cdot P_{4-7} \cdot P_{8-11} \cdot P_{12-15}}$ | $\overline{G_{12-15} + P_{12-15} \cdot G_{8-11} + P_{12-15} \cdot P_{8-11} \cdot G_{4-7} + P_{12-15} \cdot P_{8-11} \cdot P_{4-7} \cdot G_{0-3}}$ | P · C _n + G | C _{n+15} ⊕ C _{n+16} |
| 1 | S - R | ← Same as R + S Equations except substitute \bar{R}_i for R _i in definitions → | | | |
| 2 | R - S | ← Same as R + S Equations except substitute \bar{S}_i for S _i in definitions → | | | |
| 3 | R V S | LOW | HIGH | LOW | LOW |
| 4 | R ∧ S | LOW | $\overline{G_{12-15} + G_{8-11} + G_{4-7} + G_{0-3}}$ | HIGH | LOW |
| 5 | $\bar{R} \wedge S$ | LOW | Same as R ∧ S except substitute \bar{R} for R in definition | HIGH | LOW |
| 6 | R ⊕ S | $\overline{P_{0-3} \cdot P_{4-7} \cdot P_{8-11} \cdot P_{12-15}}$ | HIGH | LOW | LOW |
| 7 | $\overline{R \oplus S}$ | Same as R ⊕ S except Substitute \bar{R} for R in Definitions | HIGH | LOW | LOW |

Note: 1) + = OR



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FUNCTIONAL TABLES

| Mnemonic | MICRO CODE | | | | ALU SOURCE OPERANDS | |
|----------|----------------|----------------|----------------|------------|---------------------|---|
| | I ₂ | I ₁ | I ₀ | Octal Code | R | S |
| AQ | L | L | L | 0 | A | Q |
| AB | L | L | H | 1 | A | B |
| ZQ | L | H | L | 2 | 0 | Q |
| ZB | L | H | H | 3 | 0 | B |
| ZA | H | L | L | 4 | 0 | A |
| DA | H | L | H | 5 | D | A |
| DQ | H | H | L | 6 | D | Q |
| DZ | H | H | H | 7 | D | 0 |

Table 1: ALU Source Operand Control.

| Mnemonic | MICRO CODE | | | | ALU Function | SYMBOL |
|----------|----------------|----------------|----------------|------------|--------------|-------------------------|
| | I ₅ | I ₄ | I ₃ | Octal Code | | |
| ADD | L | L | L | 0 | R Plus S | R + S |
| SUBR | L | L | H | 1 | S Minus R | S - R |
| SUBS | L | H | L | 2 | R Minus S | R - S |
| OR | L | H | H | 3 | R OR S | R ∨ S |
| AND | H | L | L | 4 | R AND S | R ∧ S |
| NOTRS | H | L | H | 5 | R AND S | $\overline{R \wedge S}$ |
| EXOR | H | H | L | 6 | R EXOR S | R ⊕ S |
| EXNOR | H | H | H | 7 | R EX-NOR S | $\overline{R \oplus S}$ |

Table 2. ALU Function Control.

| Mnemonic | MICRO CODE | | | | RAM FUNCTION | | Q-REG. FUNCTION | | Y OUTPUT | RAM SHIFTER | | Q SHIFTER | |
|----------|----------------|----------------|----------------|------------|--------------|---------|-----------------|---------|----------|------------------|-------------------|-----------------|------------------|
| | I ₈ | I ₇ | I ₆ | Octal Code | SHIFT | LOAD | SHIFT | LOAD | | RAM ₀ | RAM ₁₅ | Q ₀ | Q ₁₅ |
| QREG | L | L | L | 0 | X | NONE | NONE | F → Q | F | X | X | X | X |
| NOP | L | L | H | 1 | X | NONE | X | NONE | F | X | X | X | X |
| RAMA | L | H | L | 2 | NONE | F → B | X | NONE | A | X | X | X | X |
| RAMF | L | H | H | 3 | NONE | F → B | X | NONE | F | X | X | X | X |
| RAMQD | H | L | L | 4 | DOWN | F/2 → B | DOWN | Q/2 → Q | F | F ₀ | IN ₁₅ | Q ₀ | IN ₁₅ |
| RAMD | H | L | H | 5 | DOWN | F/2 → B | X | NONE | F | F ₀ | IN ₁₅ | Q ₀ | X |
| RAMQU | H | H | L | 6 | UP | 2F → B | UP | 2Q → Q | F | IN ₀ | F ₁₅ | IN ₀ | Q ₁₅ |
| RAMU | H | H | H | 7 | UP | 2F → B | X | NONE | F | IN ₀ | F ₁₅ | X | Q ₁₅ |

X = Don't care.

B = Register Addressed by B inputs.

DOWN is toward LSB. UP is toward MSB.

Table 3. ALU Destination Control.

| I ₅₄₃ (Octal Code) | ALU Function | I ₂₁₀ (Octal Code) | | | | | | | |
|----------------------------------|---|-------------------------------|-------------------------|----------------|----------------|----------------|-------------------------|-------------------------|----------------|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | ALU Source (R, S) | | | | | | | |
| | | A, Q | A, B | O, Q | O, B | O, A | D, A | D, Q | D, O |
| 0 | C _n = L R Plus S C _n = H | A + Q | A + B | Q | B | A | D + A | D + Q | D |
| | | A + Q + 1 | A + B + 1 | Q + 1 | B + 1 | A + 1 | D + A + 1 | D + Q + 1 | D + 1 |
| 1 | C _n = L S Minus R C _n = H | Q - A - 1 | B - A - 1 | Q - 1 | B - 1 | A - 1 | A - D - 1 | Q - D - 1 | - D - 1 |
| | | Q - A | B - A | Q | B | A | A - D | Q - D | - D |
| 2 | C _n = L R Minus S C _n = H | A - Q - 1 | A - B - 1 | - Q - 1 | - B - 1 | - A - 1 | D - A - 1 | D - Q - 1 | D - 1 |
| | | A - Q | A - B | - Q | - B | - A | D - A | D - Q | D |
| 3 | R OR S | A ∨ Q | A ∨ B | Q | B | A | D ∨ A | D ∨ Q | D |
| 4 | R AND S | A ∧ Q | A ∧ B | 0 | 0 | 0 | D ∧ A | D ∧ Q | 0 |
| 5 | \overline{R} AND S | $\overline{A} \wedge Q$ | $\overline{A} \wedge B$ | Q | B | A | $\overline{D} \wedge A$ | $\overline{D} \wedge Q$ | 0 |
| 6 | R EX-OR S | A ⊕ Q | A ⊕ B | Q | B | A | D ⊕ A | D ⊕ Q | D |
| 7 | REX-NORS | $\overline{A \oplus Q}$ | $\overline{A \oplus B}$ | \overline{Q} | \overline{B} | \overline{A} | $\overline{D \oplus A}$ | $\overline{D \oplus Q}$ | \overline{D} |

+ = Plus; - = Minus; ∨ = OR; ∧ = AND; ⊕ = EX-OR.

Table 4. Source Operand and ALU Function Matrix.



SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0, I1 and I2 instruction inputs. The ALU performs eight functions; three arithmetic and five logic. This function selection is controlled by the I3, I4 and I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operations which the WS59016 can perform and Table 6 shows the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (CN = 0) are defined in these operations.

| Octal I543, I210 | Group | Function |
|------------------|--------|-------------------------|
| 4 0 | AND | $A \wedge Q$ |
| 4 1 | | $A \wedge B$ |
| 4 5 | | $D \wedge A$ |
| 4 6 | | $D \wedge Q$ |
| 3 0 | OR | $A \vee Q$ |
| 3 1 | | $A \vee B$ |
| 3 5 | | $D \vee A$ |
| 3 6 | | $D \vee Q$ |
| 6 0 | EX-OR | $A \nabla Q$ |
| 6 1 | | $A \nabla B$ |
| 6 5 | | $D \nabla A$ |
| 6 6 | | $D \nabla Q$ |
| 7 0 | EX-NOR | $\overline{A \nabla Q}$ |
| 7 1 | | $\overline{A \nabla B}$ |
| 7 5 | | $\overline{D \nabla A}$ |
| 7 6 | | $\overline{D \nabla Q}$ |
| 7 2 | INVERT | \overline{Q} |
| 7 3 | | \overline{B} |
| 7 4 | | \overline{A} |
| 7 7 | | \overline{D} |
| 6 2 | PASS | Q |
| 6 3 | | B |
| 6 4 | | A |
| 6 7 | | D |
| 3 2 | PASS | Q |
| 3 3 | | B |
| 3 4 | | A |
| 3 7 | | D |
| 4 2 | "ZERO" | 0 |
| 4 3 | | 0 |
| 4 4 | | 0 |
| 4 7 | | 0 |
| 5 0 | MASK | $\overline{A} \wedge Q$ |
| 5 1 | | $\overline{A} \wedge B$ |
| 5 5 | | $\overline{D} \wedge A$ |
| 5 6 | | $\overline{D} \wedge Q$ |

Table 5. ALU Logic Mode Functions.

| Octal I543, I210 | Cn = L | | Cn = H | |
|------------------|----------------------|-----------|----------------------|-----------|
| | Group | Function | Group | Function |
| 0 0 | ADD | A + Q | ADD plus one | A + Q + 1 |
| 0 1 | | A + B | | A + B + 1 |
| 0 5 | | D + A | | D + A + 1 |
| 0 6 | | D + Q | | D + Q + 1 |
| 0 2 | PASS | Q | Increment | Q + 1 |
| 0 3 | | B | | B + 1 |
| 0 4 | | A | | A + 1 |
| 0 7 | | D | | D + 1 |
| 1 2 | Decrement | Q - 1 | PASS | Q |
| 1 3 | | B - 1 | | B |
| 1 4 | | A - 1 | | A |
| 2 7 | | D - 1 | | D |
| 2 2 | 1's Comp. | -Q - 1 | 2's Comp. (Negate) | -Q |
| 2 3 | | -B - 1 | | -B |
| 2 4 | | -A - 1 | | -A |
| 1 7 | | -D - 1 | | -D |
| 1 0 | Subtract (1's Comp.) | Q - A - 1 | Subtract (2's Comp.) | Q - A |
| 1 1 | | B - A - 1 | | B - A |
| 1 5 | | A - D - 1 | | A - D |
| 1 6 | | Q - D - 1 | | Q - D |
| 2 0 | | A - Q - 1 | | A - Q |
| 2 1 | | A - B - 1 | | A - B |
| 2 5 | | D - A - 1 | | D - A |
| 2 6 | | D - Q - 1 | | D - Q |

Table 6. ALU Arithmetic Mode Functions.

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COMPETITIVE TIMING ANALYSIS

The following analysis compares the critical timing paths of a WS59016D vs. the equivalent Bipolar circuit implementation using four 2901C's and one 2902A.

As can be seen from this comparison, the WS59016 operates faster than even the theoretically achievable values of the Bipolar implementation. The actual values for the Bipolar circuit will be lengthened by the layout dependent interconnect delays between the individual devices. When these delays are taken into account, the WS59016 speed advantage becomes even greater.

TIMING COMPARISON

WS59016E vs 2901C w/2902A (Commercial)

| DATA PATH | CONTROL PATH |
|--|---|
| <p><u>2901C w/ 2902A</u></p> <p>A, B Address → \bar{P} or \bar{G} = 37ns \bar{P} or \bar{G} → C = 9ns C → F = 0, RAM_{0,15} = 25ns interconnect delay → = Xns <u>Total Delay → > 71ns</u></p> | <p><u>2901C w/ 2902A</u></p> <p>I₀₁₂ → \bar{P} or \bar{G} = 37ns \bar{P} or \bar{G} → C = 9ns C → F = 0, RAM_{0,15} = 25ns interconnect delay → = Xns <u>Total Delay → > 71ns</u></p> |
| <p><u>59016E</u></p> <p>A, B Address → F = 0, RAM_{0,15} = 55 ns interconnect delay → = 0ns <u>Total Delay → ≤ 55 ns</u></p> | <p><u>59016E</u></p> <p>I₀₁₂ → F = 0, RAM_{0,15} = 43 ns interconnect delay → = 0ns <u>Total Delay → ≤ 43 ns</u></p> |

TIMING COMPARISON

WS59016C vs 2901C w/2902A (Military)

| DATA PATH | CONTROL PATH |
|---|--|
| <p><u>2901C w/ 2902A</u></p> <p>A, B Address → \bar{P} or \bar{G} = 44ns \bar{P} or \bar{G} → C = 11.5ns C → F = 0, RAM_{0,15} = 28ns interconnect delay → = Xns <u>Total Delay → > 83.5ns</u></p> | <p><u>2901C w/ 2902A</u></p> <p>I₀₁₂ → \bar{P} or \bar{G} = 44ns \bar{P} or \bar{G} → C = 11.5ns C → F = 0, RAM_{0,15} = 28ns interconnect delay → = Xns <u>Total Delay → > 83.5ns</u></p> |
| <p><u>59016C</u></p> <p>A, B Address → F₁₅, RAM_{0,15} = 83 ns interconnect delay → = 0ns <u>Total Delay → ≤ 83ns</u></p> | <p><u>59016C</u></p> <p>I₀₁₂ → F₁₅, RAM_{0,15} = 72 ns interconnect delay → = 0ns <u>Total Delay → ≤ 72 ns</u></p> |

NOTE: This competitive analysis holds true for any 16 bit system which performs arithmetic operations. If arithmetic operations are not used, the Bipolar circuit can run faster than noted above.

COMMERCIAL RANGE AC CHARACTERISTICS (WS59016C)

The tables shown here specify the guaranteed performance of the WS59016C over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

| | |
|---|-------|
| READ-MODIFY-WRITE (from select of A, B registers to end of cycle) | 67ns |
| Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632) | 15MHz |
| Minimum Clock Low Time | 33ns |
| Minimum Clock High Time | 33ns |
| Minimum Clock Period | 67ns |

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with $C_L = 5\text{pF}$ and measured to 0.5V change of output voltage.

| | |
|--|------|
| From $\overline{\text{OE}}$ Low to Y output enable | 25ns |
| From $\overline{\text{OE}}$ High to output disable | 25ns |

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COMBINATIONAL PROPAGATION DELAYS (CL = 50PF)

| FROM OUTPUT TO OUTPUT | Y | F15 | $C_n + 16$ | $\overline{G}, \overline{P}$ | F = 0 | OVR | RAM0, RAM15 | Q0, Q15 | UNITS |
|---------------------------|----|-----|------------|------------------------------|-------|-----|----------------|------------|-------|
| A, B ADDRESS | 69 | 69 | 60 | 68 | 71 | 69 | 71 | - | ns |
| D0-D15 | 55 | 55 | 45 | 50 | 55 | 55 | 55 | - | |
| C_n | 38 | 38 | 27 | - | 42 | 38 | 42 | - | |
| I_{012} | 60 | 60 | 55 | 55 | 60 | 60 | 60 | - | |
| I_{345} | 60 | 60 | 55 | 55 | 60 | 60 | 60 | - | |
| I_{678} | 30 | - | - | - | - | - | 27 | 26 | |
| A BYPASS ALU (I = 2XX) | 45 | - | - | - | - | - | - | - | |
| CLOCK | 65 | 65 | 65 | 65 | 55 | 65 | 70 | 30 | |

| INPUT CP | Set Up before H → L | Hold after H → L | Set Up before L → H | Hold after L → H | UNITS |
|------------------------|---------------------|------------------------|---------------------|------------------|-------|
| A, B Source Address | 15 | 2 (Note 3) | 65 (Note 4) | 1 | ns |
| B Destination Address | 15 | DO NOT CHANGE (Note 2) | | 1 | |
| D0-D15 | - | - | 50 | 0 | |
| C_n | - | - | 34 | 0 | |
| I_{012} | - | - | 55 | 0 | |
| I_{345} | - | - | 55 | 0 | |
| I_{678} | 15 | DO NOT CHANGE (Note 2) | | 0 | |
| RAM0, 15 and Q0, 15 | - | - | 20 | 4 | |

- NOTES:
- 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
 - 2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
 - 3) Prior to clock H > L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
 - 4) Set-up time before H > L included here.

MILITARY RANGE AC CHARACTERISTICS (WS59016C)

The tables shown here specify the guaranteed performance of the WS59016C over the Military operating temperature range of -55°C to $+125^{\circ}\text{C}$ and a power supply range of $5\text{V} \pm 10\%$. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

| | |
|---|---------|
| READ-MODIFY-WRITE (from select of A, B registers to end of cycle) | 80ns |
| Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632) | 12.5MHz |
| Minimum Clock Low Time | 39ns |
| Minimum Clock High Time | 39ns |
| Minimum Clock Period | 80ns |

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with $C_L = 5\text{pF}$ and measured to 0.5V change of output voltage.

| | |
|--|------|
| From $\overline{\text{OE}}$ Low to Y output enable | 30ns |
| From $\overline{\text{OE}}$ High to output disable | 30ns |

COMBINATIONAL PROPAGATION DELAYS ($C_L = 50\text{PF}$)

| FROM OUTPUT \ TO OUTPUT | Y | F15 | $C_n + 16$ | $\overline{G}, \overline{P}$ | F = 0 | OVR | RAM0, RAM15 | Q0, Q15 | UNITS |
|-------------------------|----|-----|------------|------------------------------|-------|-----|-------------|---------|-------|
| A, B ADDRESS | 83 | 83 | 72 | 82 | 83 | 83 | 83 | - | ns |
| D0-D15 | 66 | 66 | 54 | 60 | 66 | 66 | 66 | - | |
| C_n | 46 | 46 | 33 | - | 53 | 46 | 53 | - | |
| I_{012} | 72 | 72 | 66 | 66 | 72 | 72 | 72 | - | |
| I_{345} | 72 | 72 | 66 | 66 | 72 | 72 | 72 | - | |
| I_{678} | 36 | - | - | - | - | - | 31 | 31 | |
| A BYPASS ALU (I = 2XX) | 55 | - | - | - | - | - | - | - | |
| CLOCK | 78 | 78 | 78 | 78 | 66 | 78 | 78 | 36 | |

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

| INPUT \ CP | Set Up before H - L | Hold after H - L | Set Up before L - H | Hold after L - H | UNITS |
|-----------------------|---------------------|------------------------|---------------------|------------------|-------|
| A, B Source Address | 20 | 2 (Note 3) | 78 (Note 4) | 2 | ns |
| B Destination Address | 20 | DO NOT CHANGE (Note 2) | | 2 | |
| D0-D15 | - | - | 60 | 0 | |
| C_n | - | - | 41 | 0 | |
| I_{012} | - | - | 66 | 0 | |
| I_{345} | - | - | 66 | 0 | |
| I_{678} | 20 | DO NOT CHANGE (Note 2) | | 0 | |
| RAM0, 15 and Q0, 15 | - | - | 25 | 5 | |

- NOTES:**
- 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
 - 2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
 - 3) Prior to clock $H > L$ transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
 - 4) Set-up time before $H > L$ included here.

COMMERCIAL RANGE AC CHARACTERISTICS (WS59016E)

The tables shown here specify the guaranteed performance of the WS59016E over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

| | |
|---|-------|
| READ-MODIFY-WRITE (from select of A, B registers to end of cycle) | 50ns |
| Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632) | 20MHz |
| Minimum Clock Low Time | 14ns |
| Minimum Clock High Time | 18ns |
| Minimum Clock Period | 47ns |

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with $C_L = 5\text{pF}$ and measured to 0.5V change of output voltage.

| | |
|--|------|
| From $\overline{\text{OE}}$ Low to Y output enable | 24ns |
| From $\overline{\text{OE}}$ High to output disable | 23ns |

COMBINATIONAL PROPAGATION DELAYS ($C_L = 50\text{pF}$)

| FROM INPUT \ TO OUTPUT | Y | F15 | C_{n+16} | $\overline{G}, \overline{P}$ | F = 0 | OVR | RAM0, RAM15 | Q0, Q15 | UNITS |
|------------------------|----|-----|------------|------------------------------|-------|-----|-------------|---------|-------|
| A, B ADDRESS | 55 | 53 | 47 | 45 | 51 | 48 | 55 | – | ns |
| D0 – D15 | 36 | 32 | 34 | 32 | 36 | 34 | 38 | – | |
| C_n | 32 | 29 | 24 | – | 32 | 28 | 32 | – | |
| I_{012} | 39 | 39 | 37 | 38 | 39 | 38 | 43 | – | |
| I_{345} | 48 | 46 | 37 | 37 | 41 | 42 | 41 | – | |
| I_{678} | 28 | – | – | – | – | – | 34 | 34 | |
| A BYPASS ALU (I = 2XX) | 36 | – | – | – | – | – | – | – | |
| CLOCK | 44 | 39 | 38 | 45 | 43 | 40 | 45 | 38 | |

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

| INPUT \ CP | Set Up Before H → L | Hold After H → L | Set Up Before L → H | Hold After L → H | UNITS |
|-----------------------|---------------------|------------------------|---------------------|------------------|-------|
| A, B Source Address | 15 | 0 (Note 3) | 23 (Note 4) | 1 | ns |
| B Destination Address | 15 | DO NOT CHANGE (Note 2) | | 1 | |
| D0 – D15 | – | – | 19 | 0 | |
| C_n | – | – | 19 | 0 | |
| I_{012} | – | – | 28 | 0 | |
| I_{345} | – | – | 30 | 0 | |
| I_{678} | 15 | DO NOT CHANGE (Note 2) | | 1 | |
| RAM0, 15 and Q0, 15 | – | – | 10 | 4 | |

NOTES:

- 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
- 2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
- 3) Prior to clock H > L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
- 4) Set-up time before H > L included here.

ORDERING INFORMATION

| PART NUMBER | SPEED | PACKAGE TYPE | PACKAGE DRAWING | OPERATING TEMPERATURE RANGE | WSI MANUFACTURING PROCEDURE |
|--------------------|--------------|-------------------------------------|------------------------|------------------------------------|------------------------------------|
| WS59016CB | C | 64 Pin Ceramic Sidebrazed DIP, 0.9" | B1 | Comm'l | Standard |
| WS59016CBM | C | 64 Pin Ceramic Sidebrazed DIP, 0.9" | B1 | Military | Standard |
| WS59016CBMB | C | 64 Pin Ceramic Sidebrazed DIP, 0.9" | B1 | Military | MIL-STD-883C |
| WS59016CJ | C | 68 Pin PLDCC | J5 | Comm'l | Standard |
| WS59016CL | C | 68 Pin CLDCC | N1 | Comm'l | Standard |
| WS59016CLM | C | 68 Pin CLDCC | N1 | Military | Standard |
| WS59016CLMB | C | 68 Pin CLDCC | N1 | Military | MIL-STD-883C |
| WS59016EJ | E | 68 Pin PLDCC | J5 | Comm'l | Standard |
| WS59016EL | E | 68 Pin CLDCC | N1 | Comm'l | Standard |